Ordering number : ENN7349

CMOS IC

LC75010W

LC75010W Car Audio DSP

Overview

The LC75010W is a car audio DSP IC that integrates the signal processing required by car audio systems, A/D and D/A converters, volume control, and other functions on a single chip. It can implement a car audio system with a minimal number of external components.

Features

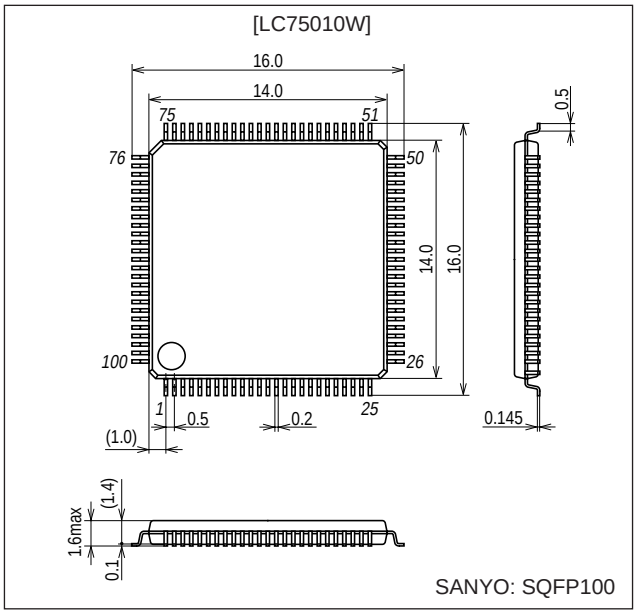
- Hardware Functions
  - — Analog source selector (BTL:1ch, OTL:3 ch)
  - — 20 bits A/D (2ch)
  - — 24 bits DSP (core, program memory, data memory)
  - — SIO (CCB I/F) (CCB is LSB first input.)
  - — 24 bits D/A (4ch)
  - — EVR (4ch)
- Software Functions* (See Note.)
  - — Bass/Mid/Treb
  - — Bal/Fad
  - — Fixed equalizer (Front/Rear/separately controlled)
  - — Loudness control
  - — Hybrid volume
  - — Anti-hard clip
  - — Dedekind (Speaton**)

  Note *: Software specifications can be modified in response to user requests.
- DSP Functions (24 fixed-point DSP)
  - — Program ROM — 8k words
  - — Data RAM — 896 words
- Supply Voltage and Package Specifications
  - — DSP core, A/D converter (digital block), D/A converter (digital block): 3.3 V
  - — A/D converter (analog block), D/A converter (analog block), volume control, crystal oscillator: 5 V
  - — Package: 100-pin SQFP (14×14 mm)

Package Dimensions

unit: mm

3181C-SQFP100



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- **CCB is Sanyo's original bus format. All bus addresses are managed by Sanyo for this format.**

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SANYO Electric Co.,Ltd. Semiconductor Company

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Pin name	Ratings			Unit
			min	typ	max	
Supply voltage (A/D, D/A, volume, etc)	V_{DDmax1}	AV_{DD1}, AV_{DD2}, AV_{DD5}, AV_{DD6}, AV_{DD7}, AV_{DD8}, AV_{DD9}, AV_{DD10}, AV_{DD11}, AV_{DD12}	–0.3		+6.0	V
Supply voltage (crystal oscillator)	V_{DDmax2}	XV_{DD}	–0.3		+6.0	V
Supply voltage (DSP core block)(I/O I/F, PLL block)	V_{DDmax3}	DV_{DD1}, DV_{DD2}, DV_{DD3}, DV_{DD4}, DV_{DD5}, DV_{DD6}, AV_{DD4}	–0.3		+4.0	V
Maximum input voltage (A/D, D/A, volume, etc)	$V_{IN}1$	AINRP1, AINRN1, AINLP1, AINLN1, AINRP2,AINLP2, AINRP3, AINLP3, AINRP4, AINLP4, VFLI, VFRI, VRLI, VRRI	–0.3		V_{DDmax1} + 0.3 (max +6.0 V)	V
Maximum input voltage (DSP core block) (I/O I/F block)	$V_{IN}2$	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7, TEST8, TEST9, TEST10, TEST13, TEST14, PWDB	–0.3		V_{DDmax3} + 0.3 (max +4.0 V)	V
	$V_{IN}3$	CL, CE, DI, RSTB, INTB	–0.3		+6.0	V
Allowable power dissipation	Pdmax	(Conditions: Audio disabled operating state, Std. Board installation ; See note)			830	mW
Maximum output current	Io	DO	0		6.0	mA
Operating temperature	Topr		–40		85	°C
Storage temperature	Tstg		–55		125	°C

Note Std. board : 114.3 mm × 76.2 mm × 1.5 mm, material ; glass epoxy resin

Allowable Operating Ranges at Ta = –40 to +85°C, $V_{SS}D = V_{SS}A$ = 0 V

Parameter	Symbol	Pin name	Ratings			Unit
			min	typ	max	
Supply voltage (analog block)	AV_{DD5}	AV_{DD1}, AV_{DD2}, AV_{DD5}, AV_{DD6}, AV_{DD7}, AV_{DD8}, AV_{DD9}, AV_{DD10}, AV_{DD11}, AV_{DD12}	+4.75		+5.25	V
Supply voltage (crystal oscillator)	XV_{DD5}	XV_{DD}	+4.75		+5.25	V
Supply voltage (digital block, PLL)	$DV_{DD3.3}$	DV_{DD1}, DV_{DD2}, DV_{DD3}, DV_{DD4}, DV_{DD5}, DV_{DD6}, AV_{DD4}	+3.0		+3.6	V
High-level input voltage	V_{IHD}	PWDB, INITB, TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7, TEST8, TEST9, TEST10, TEST13, TEST14	$0.7 \times DV_{DD3.3}$		$DV_{DD3.3}$	V
	V_{IHD1}	CL, CE, DI, RSTB	$0.7 \times AV_{DD5}$		AV_{DD5}	V
Low-level input voltage	V_{ILD}	PWDB, INITB, TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7, TEST8, TEST9, TEST10, TEST13, TEST14	V_{SS}		$0.3 \times DV_{DD3.3}$	V
	V_{ILD1}	CL, CE, DI, RSTB	V_{SS}		$0.3 \times AV_{DD5}$	V
Full-scale input level		AINRP1, AINRN1, AINLP1, AINLN1, AINRP2, AINLP2, AINRP3, AINLP3, AINRP4, AINLP4			$0.4 \times AV_{DD5}$	Vp-p
Crystal oscillator frequency *		X_{IN}, X_{OUT}		16.9344		MHz

Note*: Consult with the manufacturer of the crystal oscillator element used to verify that the circuit constant values are appropriate for that crystal oscillator element before using this circuit.

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Pin name	Ratings			Unit
			min	typ	max	
High-level input current	I_{IH}	PWDB, RSTB, INTB, CE, CL, DI, TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7, TEST8, TEST9, TEST10, TEST13, TEST14			5	µA
Low-level input current	I_{IL}	PWDB, RSTB, INTB, CE, CL, DI, TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7, TEST8, TEST9, TEST10, TEST13, TEST14	–5			µA
High-level output voltage	V_{OH}	BUSY, DO, TEST11, TEST12 (Microcontroller: 5 V)	4.5		5.5	V
		BUSY, DO, TEST11, TEST12 (Microcontroller: 3.3 V)	3.0		3.6	V
Low-level output voltage	V_{OL}	BUSY, DO, TEST11, TEST12			0.5	V
Analog output level	V_{OUT}	A_{OUT1}, A_{OUT2}, A_{OUT3}, A_{OUT4}		$0.6 \times AV_{DD5}$		V_{P-P}
Reference voltage output	Vref1 Vref2 Vref3	Vref1, Vref2, Vref3	2.35	2.5	2.65	V
Current drain	I_{AVDD5}	(Conditions: Audio disabled operating state, Std. board installed ; See note) $A_{VDD5} = X_{VDD5} = 5V$, $D_{VDD3.3} = 3.3$ V		55	72	mA
	I_{XVDD5}	(Conditions: Audio disabled operating state, Std. board installed ; See note) $A_{VDD5} = X_{VDD5} = 5V$, $D_{VDD3.3} = 3.3$ V		5	7	mA
	$I_{DVDD3.3}$	(Conditions: Audio disabled operating state, Std. board installed ; See note) $A_{VDD5} = X_{VDD5} = 5V$, $D_{VDD3.3} = 3.3$ V		65	85	mA
Power dissipation	Pd	(Conditions: Audio disabled operating state, Std. board installed ; See note) $A_{VDD5} = X_{VDD5} = 5V$, $D_{VDD3.3} = 3.3$ V		515	680	mW

Note Std. board : 114.3 mm × 76.2 mm × 1.5 mm, material : glass epoxy resin

LC75010W Analog Characteristics

Conditions: Analog system: 5 V, digital system: 3.3 V, fs: 44.1 kHz, signal frequency: 1 kHz, from the analog source selector input to the volume control circuit output.
Measurement band: 10 Hz to 20 kHz, using the SANYO-specified DSP evaluation board.
Test circuit: LC75010W external circuit structure with the DSP operating in through mode (4-bit shiftup), room temperature
Test equipment: Audio analyzer (Rohde & Schwarz UPD)

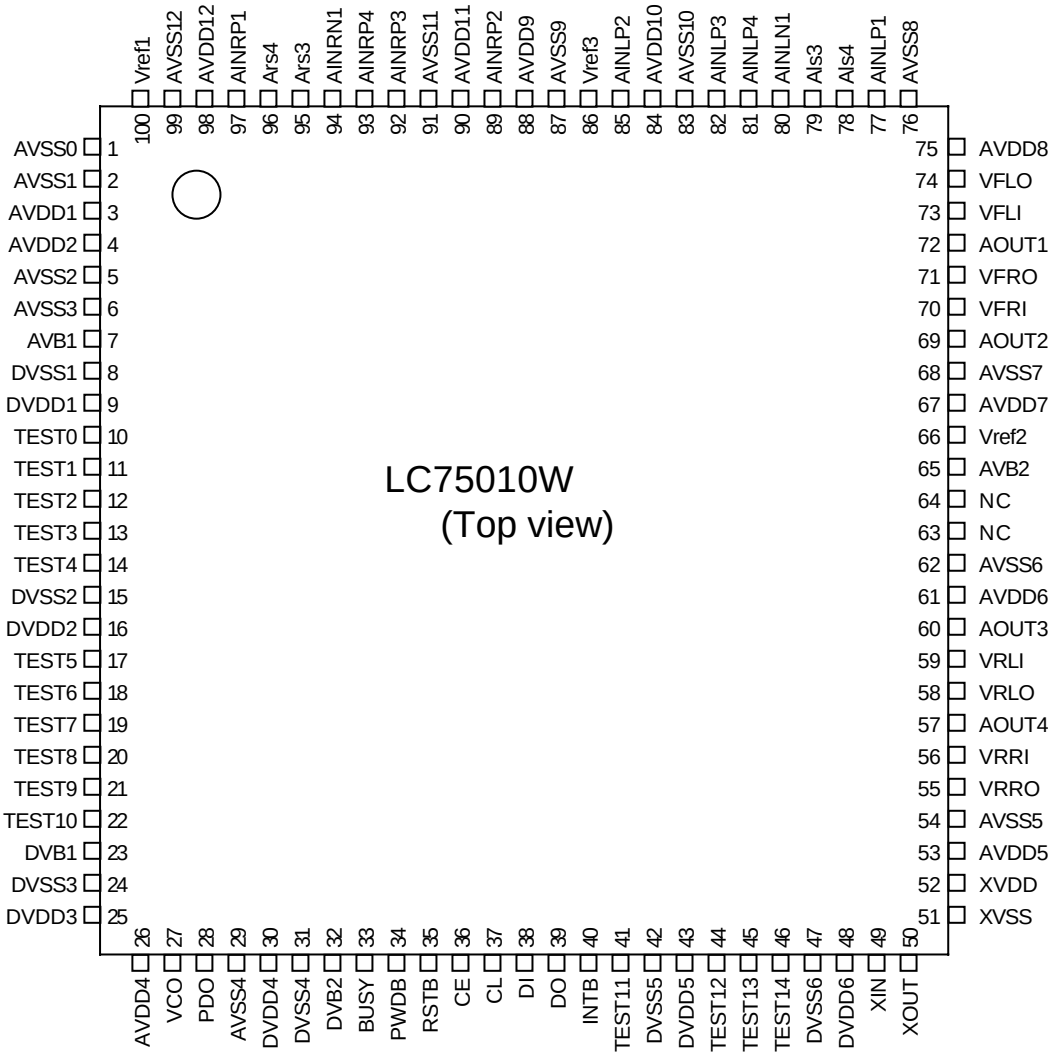
Parameter	Conditions	Ratings			Unit
		min	typ	max	
S/N	A-weighted, Input conditions: 2 Vp-p	85	90	—	dB
Dynamic range	A-weighted	85	90	—	dB
THD+N	Input conditions: 1.5 Vp-p. See note.	—	–86	–80	dB

Note: THD+N shows the optimal characteristics for an input (1.5 Vp-p) that is 3 dB lower than the full-scale input level.

CCB Timing

Parameter	Symbol	Pin name	Ratings			Unit
			min	typ	max	
Data setup time	t_{SU}	DI, CL	0.75			µs
Data hold time	t_{HD}	DI, CL	0.75			µs
Clock low-level time	t_{CL}	CL	0.75			µs
Clock high-level time	t_{CH}	CL	0.75			µs
CE wait time	t_{EL}	CE, CL	0.75			µs
CE setup time	t_{ES}	CE, CL	0.75			µs
CE hold time	t_{EH}	CE, CL	0.75			µs
Data latch change time	t_{LC}				0.75	µs
Data output time	t_{DC} t_{DH}	DO, CL DO, CE			0.35	µs

Pin Assignments



Pin Functions

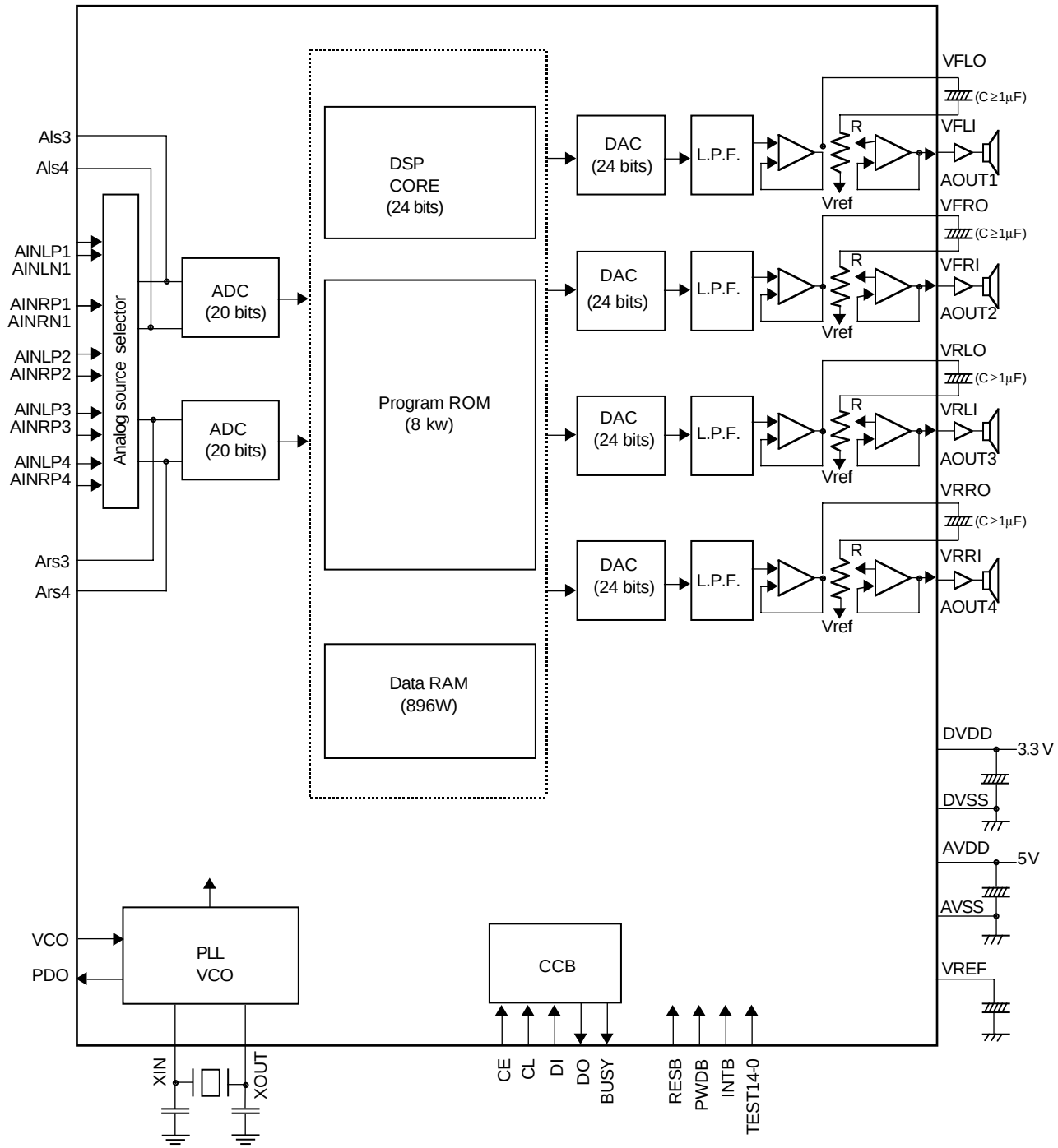
Pin No.	Pin name	Input/Output (I/O)	Function
97	AINRP1	I	Analog BTL input (Rch +)
94	AINRN1	I	Analog BTL input (Rch -)
77	AINLP1	I	Analog BTL input (Lch +)
80	AINLN1	I	Analog BTL input (Lch -)
89	AINRP2	I	Analog OTL input1 (Rch +)
85	AINLP2	I	Analog OTL input1 (Lch +)
92	AINRP3	I	Analog OTL input2 (Rch +)
82	AINLP3	I	Analog OTL input2 (Lch +)
93	AINRP4	I	Analog OTL input3 (Rch +)
81	AINLP4	I	Analog OTL input3 (Lch +)
34	PWDB	I	Standby mode (active low) Setting the PWDB pin to the low level sets the LC75010W to standby mode (also know as "power down mode"). In standby mode, the DSP system clock and the crystal oscillator are stopped and the whole LC75010W goes to the stopped state. This pin must be held at the high level during normal operation.
35	RSTB	I	Reset (active low) A reset is normally applied at power on, after recovering from a temporary power outage, and after returning from standby mode ("power down mode").
40	INTB	I	Interrupt (active low) (Software clip input (0/1)) Provides feedback control to the DSP to prevent clipping when an overflow occurs in the amplifier output.
10	TEST0	I/O	Test pin
11	TEST1	I/O	Test pin
12	TEST2	I/O	Test pin
13	TEST3	I/O	Test pin
14	TEST4	I/O	Test pin
17	TEST5	I/O	Test pin
18	TEST6	I/O	Test pin
19	TEST7	I/O	Test pin
20	TEST8	I/O	Test pin
21	TEST9	I/O	Test pin
22	TEST10	I/O	Test pin
41	TEST11	I/O	Test pin
44	TEST12	I/O	Test pin
45	TEST13	I/O	Test pin
46	TEST14	I/O	Test pin
49	XIN	I	Crystal input (384 fs = 16.9344 MHz) (fs = 44.1 kHz)
50	XOUT	O	Crystal output
27	VCO	I	VCO control
28	PDO	O	Charge pump output
36	CE	I	CCB enable
37	CL	I	CCB clock
38	DI	I	Data in
39	DO	O	Data out
33	BUSY	O	CCB ready monitor Outputs the state of the DSP CCB receive buffer. A low-level output from the BUSY pin indicates that the buffer is empty. A high-level output indicates that command data is present in the receive buffer.
74	VFLO	O	Volume front Lch output
73	VFLI	I	Volume front Lch input
71	VFRO	O	Volume front Rch output
70	VFRI	I	Volume front Rch input
58	VRLO	O	Volume rear Lch output
59	VRLI	I	Volume rear Lch input
55	VRRO	O	Volume rear Rch output
56	VRRI	I	Volume rear Rch input

Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Input/Output (I/O)	Function
100	Vref1		Reference voltage
66	Vref2		Reference voltage
86	Vref3		Reference voltage
72	AOUT1	O	Analog out 1
69	AOUT2	O	Analog out 2
60	AOUT3	O	Analog out 3
57	AOUT4	O	Analog out 4
9	$DV_{DD}1$		Digital V_{DD} (3.3 V)
16	$DV_{DD}2$		Digital V_{DD} (3.3 V)
25	$DV_{DD}3$		Digital V_{DD} (3.3 V)
30	$DV_{DD}4$		Digital V_{DD} (3.3 V)
43	$DV_{DD}5$		Digital V_{DD} (3.3 V)
48	$DV_{DD}6$		Digital V_{DD} (3.3 V)
8	$DV_{SS}1$		Digital V_{SS}
15	$DV_{SS}2$		Digital V_{SS}
24	$DV_{SS}3$		Digital V_{SS}
31	$DV_{SS}4$		Digital V_{SS}
42	$DV_{SS}5$		Digital V_{SS}
47	$DV_{SS}6$		Digital V_{SS}
29	$AV_{SS}4$		Digital V_{SS}
23	DVB1		Digital board GND
32	DVB2		Digital board GND
3	$AV_{DD}1$		Analog V_{DD} (5 V)
4	$AV_{DD}2$		Analog V_{DD} (5 V)
53	$AV_{DD}5$		Analog V_{DD} (5 V)
61	$AV_{DD}6$		Analog V_{DD} (5 V)
67	$AV_{DD}7$		Analog V_{DD} (5 V)
75	$AV_{DD}8$		Analog V_{DD} (5 V)
88	$AV_{DD}9$		Analog V_{DD} (5 V)
84	$AV_{DD}10$		Analog V_{DD} (5 V)
90	$AV_{DD}11$		Analog V_{DD} (5 V)
98	$AV_{DD}12$		Analog V_{DD} (5 V)
26	$AV_{DD}4$		Digital V_{DD} (3.3 V)
1	$AV_{SS}0$		Analog V_{SS}
2	$AV_{SS}1$		Analog V_{SS}
5	$AV_{SS}2$		Analog V_{SS}
6	$AV_{SS}3$		Analog V_{SS}
54	$AV_{SS}5$		Analog V_{SS}
62	$AV_{SS}6$		Analog V_{SS}
68	$AV_{SS}7$		Analog V_{SS}
76	$AV_{SS}8$		Analog V_{SS}
87	$AV_{SS}9$		Analog V_{SS}
83	$AV_{SS}10$		Analog V_{SS}
91	$AV_{SS}11$		Analog V_{SS}
99	$AV_{SS}12$		Analog V_{SS}
7	AVB1		Analog Board GND
65	AVB2		Analog Board GND
52	XV_{DD}		OSC V_{DD} (5 V)
51	XV_{SS}		OSC V_{SS}
95	Ars3		Analog Rch source control
96	Ars4		Analog Rch source control
79	Als3		Analog Lch source control
78	Als4		Analog Lch source control

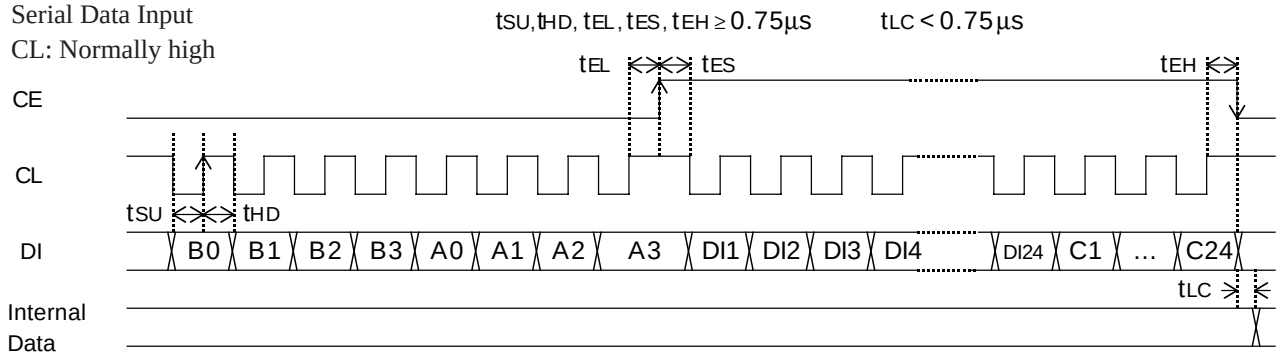
Block Diagram



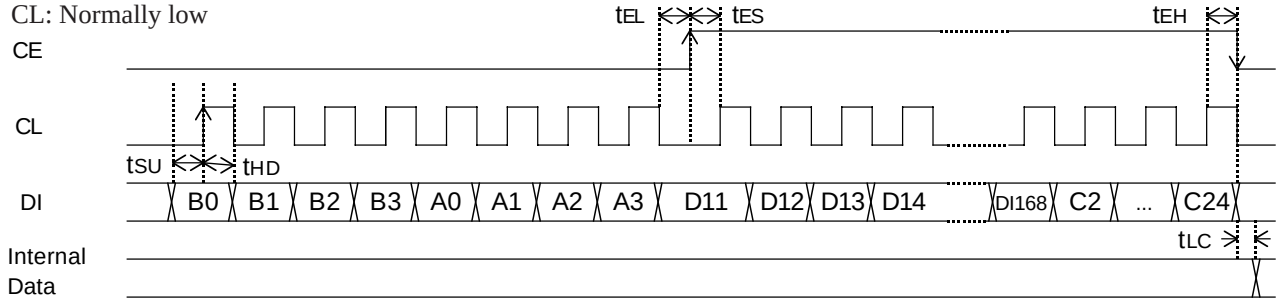
CCB Control System Timing and Data Format

The LC75010W uses a CCB (Computer Control Bus) serial bus, which is a SANYO-developed bus format.
The input serial data consists of a total of (8 + DI + C) bits. Here, the first 8 bits are the CCB address, the next DI bits are the data bits, and the last C bits are control bits. The output serial data consists of (8 + DO) bits. Here, the first 8 bits are the CCB address and the next DO bits are the output data bits. Serial data can be input or output after power has been applied, the crystal oscillator and PLL circuits have stabilized, and a reset has been applied.

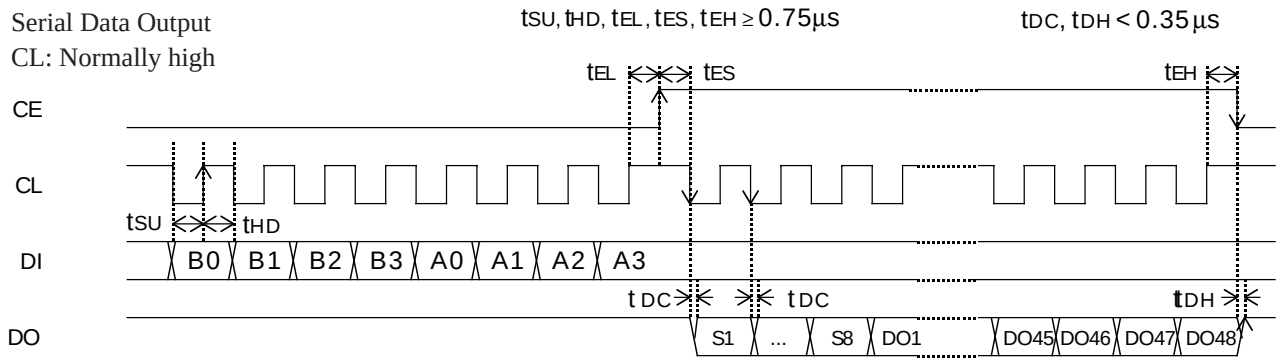
- Serial Data Input
  CL: Normally high



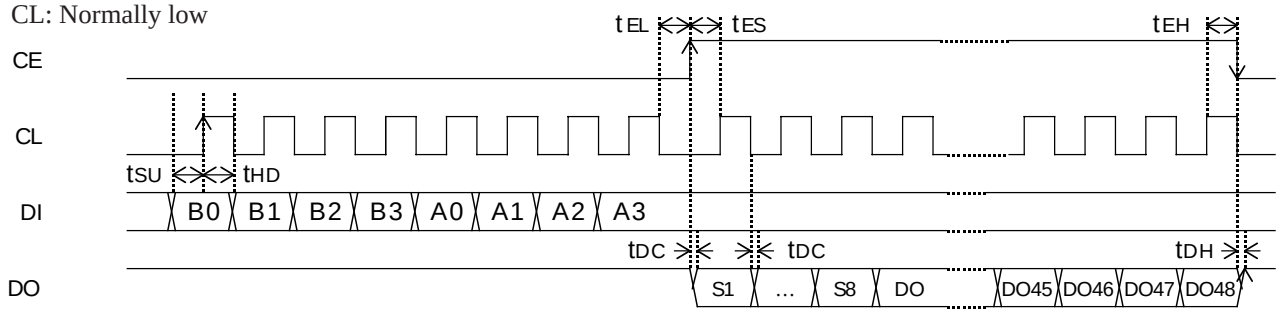
CL: Normally low



- Serial Data Output
  CL: Normally high

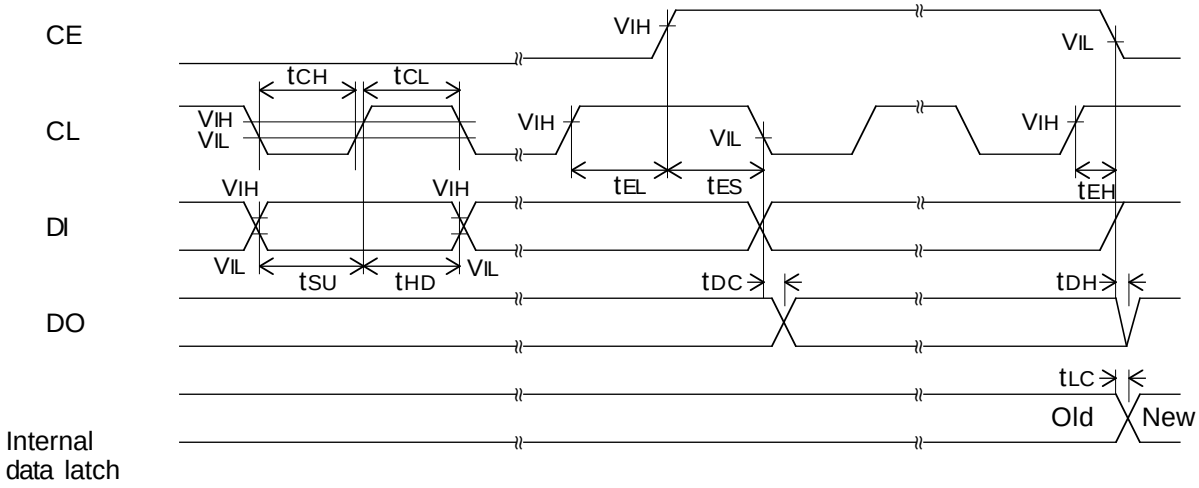


CL: Normally low



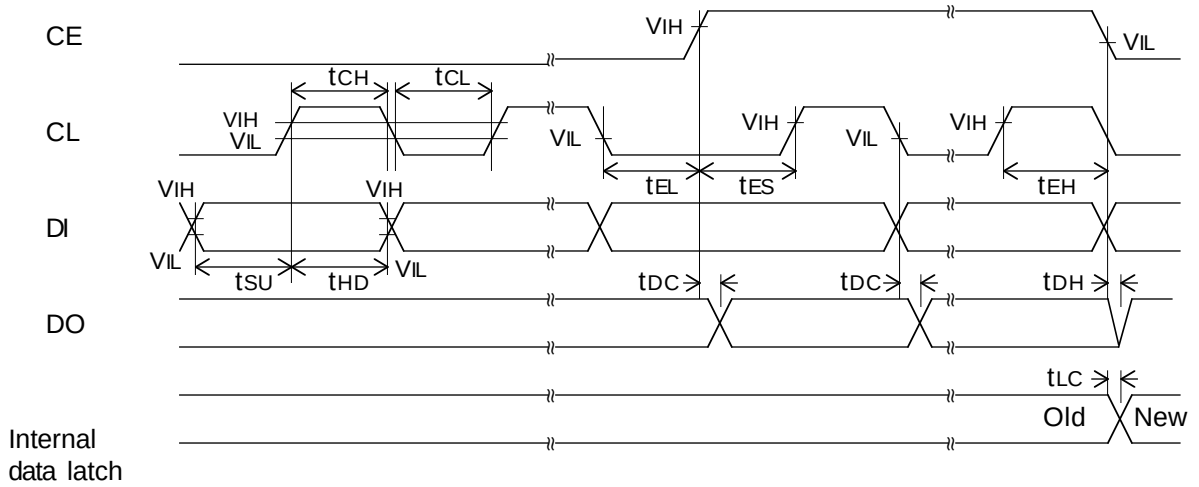
Note: Since the DO pin is an n-channel open-drain output, the data transition times (tDC and tDH) differ depending on the value of the pull-up resistor used.

• Serial Data Timing
CL: Normally high



When CL is stopped at the high level

CL: Normally low



When CL is stopped at the low level

Reset Timing

After power has been applied, and after crystal oscillator operation and PLL circuit operation have stabilized, a reset must be applied at the point that the Vref voltages (Vref1, Vref2, and Vref3) exceed the minimum level of 2.35 V. The reset period must be set up to include a period of at least 0.5 µs during which the reset signal is held fixed at the low level. Audio processing (audio input/audio output) cannot be performed during the A/D converter calibration period (100 ms), which directly follows the reset.

Note on Changes to the DSP Core Main Clock

The LC75010W DSP core main clock can be switched by setting the TEST8 pin either low or high as shown below.

TEST8	DSP core main clock (Crystal oscillator: 16.9344 MHz)
Low (DV_{SS})	38.1024 MHz
High (DV_{DD} 3.3)	40.2192 MHz

Notes on Filter Coefficient Settings (precision of calculations)

The IIR filter calculations are performed using 24-bit coefficients, 24-bit delay functions, 24 × 24 = 48-bit multiplications, and 48 + 48 = 48-bit additions.

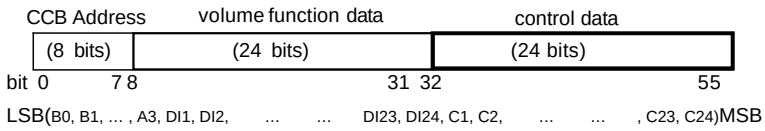
For certain values of the filter coefficients, the precision can become inadequate during the process of the filter calculation. Such errors can result in switching noise occurring when changing between different steps in the volume control.

*: This problem can occur when setting the second-order IIR with filter coefficients having low characteristic frequencies (for example, the cutoff frequency or the center frequency). For example, switching noise will occur if the coefficients for a high-pass filter with a cutoff frequency of 25 Hz and a Q of 0.7 are set with FixEQ.)
The following workaround can be effective if switching noise occurs due to second-order IIR filter coefficient settings.

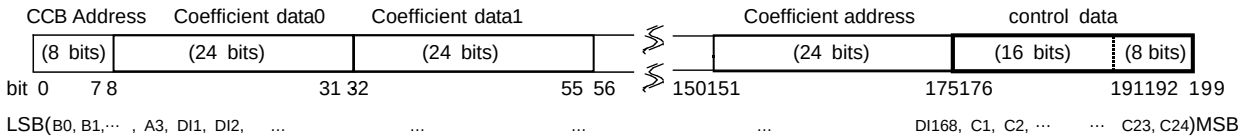
- Increase the characteristic frequency without changing the second-order characteristics, for example, increase the cutoff frequency from 25 Hz to 100 Hz.
- Use the second-order characteristics as the first-order characteristics and define the coefficients for first-order characteristics.

- Serial Input Data Format Examples

Example 1: Data format for the volume function

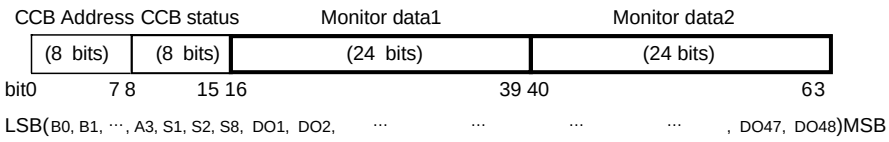


Example 2: Data format for 24-bit coefficient data (Total: 200 bits maximum)

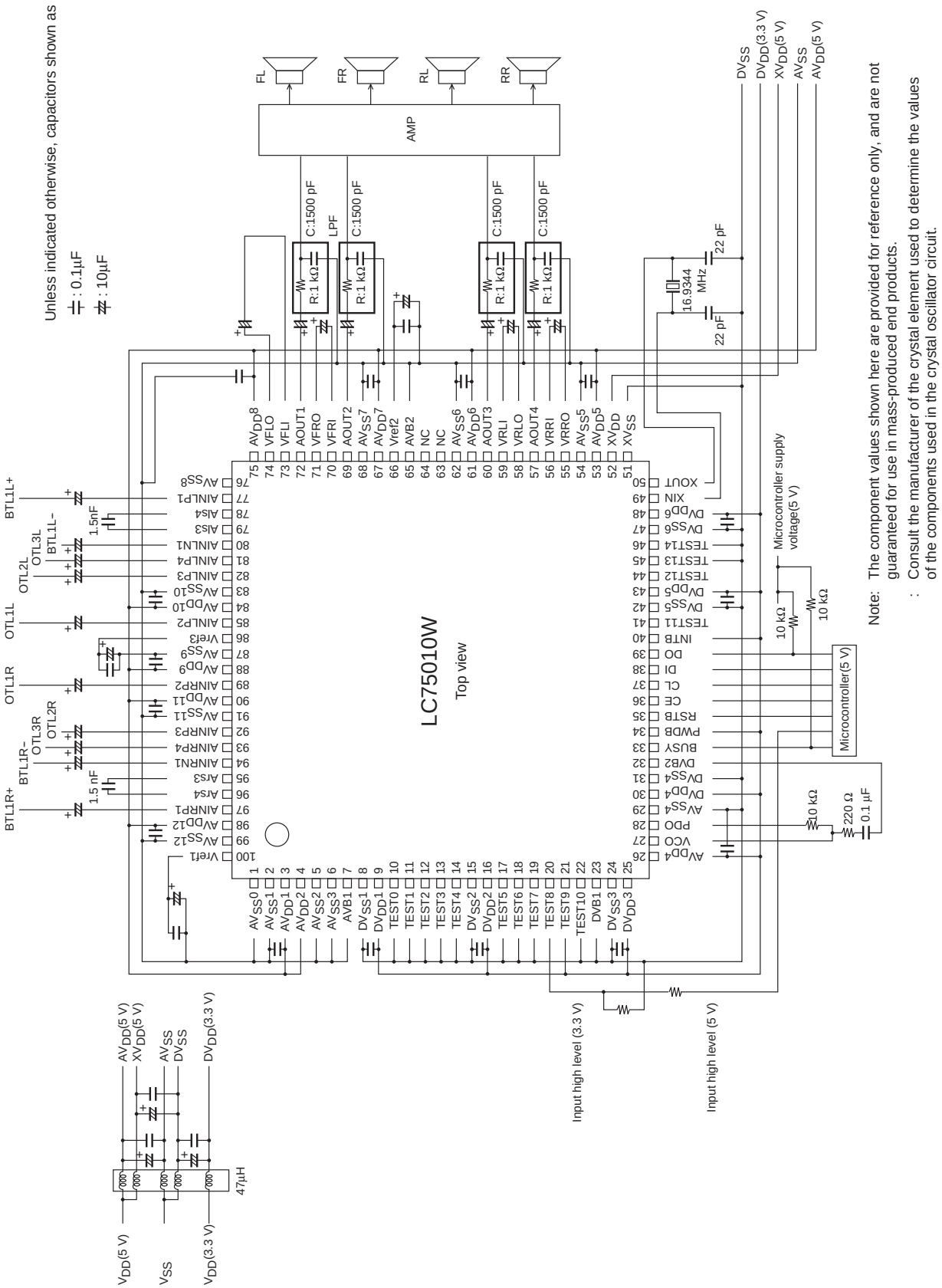


- Serial Output Data Format Example

Example 1: CCB status register format (Total: 64 bits)



Peripheral Circuit Example



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